

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)
2. (Currently Amended) A method ~~as claimed in claim 1~~ of operating a data-processing device with an integrated circuit comprising a central processing unit (CPU) and one or more co-processors, in which the integrated circuit performs cryptographic operations characterized in that in performing a cryptographic operation in the integrated circuit, at least two processors, CPU and co-processors, perform a cryptographic operation simultaneously and in parallel, characterized in that only the cryptographic operation of one processor, CPU or co-processor, is a useful operation and all other cryptographic operations are dummy operations whose results are rejected.
3. (original) A method as claimed in claim 2, characterized in that the selection as to which processor, CPU or co-processor, performs a useful operation is random-controlled.
4. (Currently Amended) A method ~~as claimed in any one of the preceding claims of~~ operating a data-processing device with an integrated circuit comprising a central processing unit (CPU) and one or more co-processors, in which the integrated circuit performs cryptographic operations characterized in that in performing a cryptographic operation in the integrated circuit, at least two processors, CPU and co-processors, perform a cryptographic operation simultaneously and in parallel, characterized in that a cryptographic operation is split up into at least two sub-operations and in that at least two processors perform at least one sub-operation ~~the sub-operations~~ in parallel and simultaneously with at least one dummy operation whose results are rejected.
5. (Cancelled)
6. (Currently Amended) A method as claimed in claim ~~5~~ 4, characterized in that the selection as to which processor performs the at least one sub-operation in parallel and

simultaneously with at least one dummy operation ~~operation complementarily or not complementarily~~ is random-controlled.

7. (Currently Amended) A method ~~as claimed in claim 1~~ of operating a data-processing device with an integrated circuit comprising a central processing unit (CPU) and one or more co-processors, in which the integrated circuit performs cryptographic operations characterized in that in performing a cryptographic operation in the integrated circuit, at least two processors, CPU and co-processors, perform a cryptographic operation simultaneously and in parallel, characterized in that a cryptographic operation is split up into at least two sub-operations, and at least one sub-operation is the sub-operations are performed simultaneously and in parallel with at least one dummy operation by the processors, CPU and co-processors, while subsequently corresponding sub-results are combined and the at least one dummy operation results are rejected to an overall result of the overall cryptographic operation.
8. (original) A method as claimed in claim 7, characterized in that the split-up of the cryptographic operation into sub-operation is random-controlled.
9. (Currently Amended) A method as claimed in claim 7 ~~or 8~~, characterized in that the sub-operations are parts of an encryption in accordance with Data Encryption Standard (DES) ~~DES (Data Encryption Standard)~~.
10. (Currently Amended) A data-processing device, ~~particularly a chip-card or smart card, particularly for performing a method as claimed in any one of the preceding claims,~~ with an integrated circuit comprising a central processing unit (CPU) (40) and one or more co-processors (42), characterized in that the integrated circuit comprises a control unit (48, 30) which controls the processors, CPU (40) and co-processors (42) in such a way that, in the case of a cryptographic operation, at least two processors perform a

cryptographic operation simultaneously and in parallel with at least one dummy operation.

11. (Currently Amended) A data-processing device as claimed in claim 10, characterized in that the control unit comprises a splitter (18) which splits up a cryptographic operation into at least two sub-operations (20, 22) and at least one sub-operation and at least one dummy operation is supplied and supplies them for simultaneous processing to two separate processors of the integrated circuit, CPU (10) and co-processors (12).

12. (Currently Amended) A data-processing device as claimed in claim 11, characterized in that the control unit further comprises a recombiner (30) which recombines each sub-result (26, 28) of the sub-operations (20, 22) simultaneously performed by the processors (10, 12) and the at least one dummy operation results are rejected to an overall result of the overall cryptographic operation.

13. (Currently Amended) A data-processing device ~~as claimed in claim 12~~ with an integrated circuit comprising a central processing unit (CPU) and one or more co-processors, characterized in that the integrated circuit comprises a control unit which controls the processors, CPU and co-processors in such a way that, in the case of a cryptographic operation, at least two processors perform a cryptographic operation simultaneously and in parallel, the control unit comprises a splitter which splits up a cryptographic operation into at least two sub-operations and supplies them for simultaneous processing to two separate processors of the integrated circuit, CPU and co-processors, the control unit further comprises a recombiner which recombines each sub-result of the sub-operations simultaneously performed by the processors, characterized in that the splitter is formed in such a way that at least one sub-operation is a dummy operation and in that the recombiner is formed in such a way that it rejects the relevant result of a processor that has performed a dummy operation.

14. (Currently Amended) A data-processing device of claim ~~as claimed in any one of claims 11 to 13~~, characterized in that the integrated circuit additionally comprises a random generator (24) which is connected to the splitter (18) in such a way that it operates in a random-controlled manner.

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